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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/622,564	08/18/2000	Ludwig Schweiger	P00,1539	7385

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EXAMINER	
FERRIS, DERRICK W	

ART UNIT	PAPER NUMBER
2663	

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/622,564	SCHWEIGER, LUDWIG	
	Examiner	Art Unit	
	Derrick W. Ferris	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-18* is/are allowed.

6)☒ Claim(s) *1-3,5,6,8,9 and 19-26* is/are rejected.

7)☒ Claim(s) *4 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. **Claims 1-26** as amended are still in consideration for this application. Applicant has amended claims **1-9**. Applicant has canceled no claims. Applicant has added claims **10-26**.

2. Examiner does **not withdraw** the anticipated rejection to ***McDysan*** for Office action filed **11/26/03**. In addressing applicant's arguments in the response filed **03/31/04**, applicant argues the further amended limitation of the buffer memory being configured to store FR data sequences from the FR module and ATM data sequences from the ATM communications module. In particular, the issue is "data sequences". Examiner assumes a reasonable but broad interpretation of the term "data sequences" in view of applicant's specification. Specifically, examiner interprets "data sequences" to read as either the header information *or* the payload information. The interpretation is supported since the Background of applicant's specification presents the problem of storing data sequences were data sequences are in relation to the header (i.e., control) information, see e.g., bottom of page 1. Examiner also notes that applicant teaches that data sequences may contain usage data and control data, see e.g., bottom of page 2. The limitation is met since *McDysan* teaches storing control data, see e.g., figures 10 and 11 in relation to figures 12 and 13 respectively. Examiner will agree that it may not be clear where the payload information is stored in *McDysan*. The examiner would allow the rejected claims if applicant further amended the claims to further recite that the data sequences comprise of "*usage data and control data*" *and* that the information is stored in a *common* buffer memory. Examiner would like to further point out that U.S. Patent No. 6,205,152 B1 to *Von Ahnen et al.* (not used in the rejection) teaches storing usage data information and control data information in

separate memories (i.e., local memory 208 and payload memory 202 respectfully) that are distinct from a control processor 207 as shown in figure 3.

3. Examiner does **not withdraw** the obviousness rejection to ***McDysan*** in further view of ***PCI Local Bus Specifications*** for Office action filed **11/26/03**. In addressing applicant's arguments in the response filed **03/31/04**, see similar reasoning above for the anticipated rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. **Claims 1, 2, 5, 6, 8, 9, 19, 21, 22, 23 and 25-26** are rejected under 35 U.S.C. 102(e) as being anticipated by *McDysan* (US Patent No.: 6,226,260 131)

Regarding **claims 1 and 5**, in Fig. 10 *MacDysan* teaches a device for converting data between FR format and ATM format including a FR/ATM adapter 1040 (FR module and ATM

module) connected to an ATM link attached to switch 940 and a FR link 905. The claimed central computer and buffer memory read on the processor 1020 and the memory 1030, respectively. In addition, the bus 1015, an internal bus, connects the memory 1030 to the processor 1020 and the adapter 1040 as claimed. See col. 9, lines 51-58.

Regarding **claim 2**, *McDyson* teaches: "In particular, FR-IWF module 920 includes a data bus 1015" (Col. Lines 52-53) (a bus link).

Regarding **claim 6**, *McDyson* teaches: "Memory 1030 includes storage for T/R FR UNI table 1035." (Col. Lines 57-58) (comprises a reception unit and a transmission unit).

Regarding **claim 8**, refer to the explanation provided for rejecting claim 1, above. Moreover, refer to col. 10 lines 24-40 as follows: "Frame Relay InterWorking Function (FR-IWF) The operation of an FR-IWF module 920 is described with reference to FIG. 12. In particular, FIG. 12 shows the serial flow of data and status signaling from a particular FR UNI input," (reading in FR data sequences), "Rx FR-UNI, through FR-IWF 920 to a cell-switch 940. UART 1010 receives user data frames 1201 from Rx FR UNI. The user data frames 1201 include a header indicating the particular FR DLCI followed by user data information field I." (storing said read-in data in said buffer...), "Processor 1020 (and/or FR/Adapter 1040) uses the received FR-DLCI to index a row in Table 1035 having corresponding Tx ATM PHY, ATM VCC and ATM DLCI information." (controlling, with said central computer), "FR/ATM adapter 1040 segments and reassembles (SAR) the data from a frame to cell format." (converting said stored data into ATM format...), "Processor 1020 stores the Rx ATM PHY value in Table 1035 in a row based on the received ATM VCC and ATM DLCI information in the ATM-STAT message 1207. (non-interrupted operations ... buffer memory).

Regarding **claim 9**, refer to the explanation provided for rejecting claim 1, above, Moreover, *McDyson* teaches: "Considering the reverse flow of data, FR-ATM adapter 1040 also converts user data I received as one or more cells 1205 from the switch 940 into one or more frames 1206." (Col. 10, line 66 through col. 11, line 1) (reading in and desegmenting an ATM data sequence), "The received ATM VCC and ATM DLCI fields in cells 1205 are used by processor 1020 to index a row in the Table 1035" (col. 11, lines 4-8) (storing said read in...), "The FR-DLCI and corresponding received user data I are then sent in frames (1206) by UART 1010 over a Tx-FR UNI" (col. 11, lines 8-10) (reading out said same data converted into FR format...), "Processor 1020 stores the RxATM PHY value in table 1035 in a row based on the received ATM VCC and ATM DLCI information in the ATM□STAT message 1207." (Col. 11, lines 28-31) (providing non-interrupted operation ...said buffer memory).

As to **claim 19**, see similar rejection for claim 2.

As to **claim 21**, see similar rejection for claim 5.

As to **claim 22**, see similar rejection for claim 6.

As to **claim 23**, see similar rejection for claim 2.

As to **claim 25**, see similar rejection for claim 5.

As to **claim 26**, see similar rejection for claim 6.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 3, 20, and 24** is rejected under 35 U.S.C. 103(a) as being unpatentable over *McDyson* in view of *PCI Local Bus Specifications*.

Regarding **claim 3**, *McDyson* does not specify the data bus used for interconnecting the processor, memory, and the input/output devices. However, the PCI specification defines interconnecting devices on a printed circuit board as a major objective of the bus design. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains to utilize the PCI bus as the interconnecting mechanism for the integrated devices. The motivation for using a standard bus could have involved time and cost savings in addition to the user community's familiarity with such a standard.

As to **claim 20**, see similar rejection for claim 3.

As to **claim 24**, see similar rejection for claim 3.

Allowable Subject Matter

8. **Claims 4 and 7** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. **Claims 10-18** are allowable.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Derrick W. Ferris whose telephone number is (703) 305-4225. The examiner can normally be reached on M-F 9 A.M. - 4:30 P.M. E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (703) 308-5340. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Derrick W. Ferris
Examiner
Art Unit 2663

DWF

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 6/14/04